Please amend the present application as follows:

Claims

The following is a copy of Applicant' claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("~~——~~"), as is applicable:

1. (Currently Amended) A ~~phase lock loop circuit comprising a~~ low power voltage-to-current converter for use in a phase locked loop, comprising:

an input stage (450) comprising:

a pair of differential signal input terminals (402, 404) operable to receive differential input signals ~~from a charge pump~~;

first (430) and second (432) switching transistors each coupled to one of the pair of differential signal input terminals;

first (434) and second (436) complementary transistors coupled to the first and second switching transistor, respectively, the first and the second switching transistors and the first and the second complementary transistors arranged as part of a folded cascode configuration;

an output stage (452) coupled to the input stage ~~first complementary transistors~~; and

a non-differential output terminal (412) coupled to the output stage, where the output terminal is operable to transmit an output current signal as a function of ~~voltages associated with~~ the differential input signals.

2. (Currently Amended) The voltage-to-current converter ~~phase lock loop~~ converter of claim 1, where the input stage is a rail-to-rail input stage.

3. (Currently Amended) The voltage-to-current converter ~~phase lock loop~~ of claim 2, where the rail-to-rail input stage is a resistorless input stage.

4. (Currently Amended) The voltage-to-current converter ~~phase lock loop~~ of claim 1, ~~where the voltage-to-current converter comprises~~ further including a second output stage, wherein the output stage and the second output stage include a constant current source that provides a substantially constant current for the center frequency of the phase lock loop output when the difference between the differential input signals is substantially zero.

5. (Currently Amended) The voltage-to-current converter ~~phase lock loop~~ of claim 1, wherein the output stage comprises a ~~first output stage and a second output stage, the first output stage being coupled to the first complementary transistor and to the non-differential output terminal, the second output stage being coupled to the first~~ differential output stage.

6. (Currently Amended) The voltage-to-current converter ~~phase lock loop~~ of claim 5, wherein the second output stage comprises a bandgap reference circuit coupled to a bandgap reference signal and to a supply voltage.

7. (Currently Amended) The voltage-to-current converter ~~phase lock loop~~ of claim 6, wherein the bandgap reference signal is approximately 1.23 to 1.25 volts.

8. (Currently Amended) The voltage-to-current converter ~~phase lock loop~~ of claim 1, further comprising a biasing transistor coupled to a bias signal coupled to the output of a charge pump of the phase locked loop and to a supply voltage, wherein the biasing transistor is configured to generate a bias current for the first and second complementary transistors of the input stage.

9-15. (Cancelled)

16. (Newly added) The voltage-to-current converter of claim 8, wherein the bias signal is provided from the supply voltage and a voltage divider circuit of the charge pump.